AMENDED CLAIMS

1. (previously presented) A method of improving the efficiency of synchronizing a clock signal for an integrated circuit, comprising:

providing a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY);

detecting a plurality of phases of CIN and CDLY based on timing conditions associated with CIN and CDLY; and

selectively inputting CIN or CIN' into a synchronous mirror delay (SMD) based on the phase of CIN and CDLY to reduce a number of delay stages in the SMD.

2. (previously presented) The method of claim 1 wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}), and selectively inputting includes inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ to reduce the number of delay stages in the SMD.

3. (original) The method of claim 2 wherein the number of delay stages in the SMD is reduced substantially in half.

4. (previously presented) The method of claim 2 wherein the SMD has a plurality of delay lines, and the number of delay stages in at least one of the SMD delay lines is reduced substantially to 59 from 128.

5. (previously presented) A method of improving the efficiency of synchronizing a clock signal for an integrated circuit, comprising:

providing a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), each signal having timing characteristics;

interposing a phase detector and selection system between an external clock signal and a synchronous mirror delay (SMD);

determining which of a number of phases the signals are based on the timing characteristics; and

selectively directing the signals based upon the phase of the signals.

6. (previously presented) The method of claim 5 wherein selectively directing includes selectively directing CIN or CIN' to the SMD based upon the timing characteristics of CIN and CDLY.

7. (previously presented) The method of claim 5 wherein selectively directing includes bypassing CIN or CIN' from the SMD based upon the timing characteristics of CIN and CDLY.

8. (previously presented) The method of claim 5 further including defining the timing characteristics as a period of CIN as t_{ck} and defining a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein determining includes determining that the phases include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$.

9. (previously presented) A method of synchronizing a clock signal for an integrated circuit, comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN'), and a clock delay signal (CDLY) having timing characteristics;

differentiating, with a phase detector, a plurality of phases based upon the timing characteristics of CIN and CDLY; and

selecting, based on the phases, one of CIN and CIN' to be input into a synchronous mirror delay (SMD) thereby reducing a number of delay stages in the SMD.

10. (previously presented) A method of synchronizing a clock signal for an integrated circuit, comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN'), and a clock delay signal (CDLY) having timing characteristics;

determining a plurality of phases based upon the timing characteristics of CIN and CDLY; and

for at least one phase, directing CIN' into a synchronous mirror delay (SMD) such that a reduced number of delay stages are achieved.

11. (previously presented) The method of claim 10 wherein the timing characteristics define a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and directing occurs when $t_{mdl} < t_{ck}/2$.

12. (previously presented) A method of synchronizing a clock signal for an integrated circuit, comprising:

a) providing an internal clock signal (CIN), an inverted internal clock signal (CIN'), and a clock delay signal (CDLY) having timing characteristics;

b) determining a plurality of phases based upon the timing characteristics of CIN and CDLY;

c) for at least one phase, directing CIN' into a synchronous mirror delay (SMD) such that a reduced number of delay stages are achieved;

wherein the timing characteristics define a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and directing occurs when $t_{mdl} < t_{ck}/2$;

d) multiplexing an input with an input selection multiplexor to select whether to direct the CIN or CIN' into the SMD, based on the phase determined in the determining step; and

e) multiplexing, with an output selection multiplexor, an output of the input selection multiplexor with a SMD output, the output selection multiplexor selecting whether to output, based on the phase determined in the determining step, the SMD output or CIN bypassing the SMD, as an input to a clock tree to generate an internal clock signal.

13. (currently amended) ~~A memory device, comprising:~~

~~a synchronous mirror delay (SMD); and~~

~~a phase detector in electronic communication with the SMD and comprising:~~

~~means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and CDLY each having timing characteristics; and~~

~~means for outputting a pair of branches each having a logical level, the logical levels of the branches defining a plurality of conditions based on the timing characteristics of CIN and CDLY;~~

~~wherein for at least one of the plurality of conditions, the memory device comprises means for reducing a number of delay stages for a selected signal to pass through the SMD based on one of the plurality of conditions.~~

A memory device, comprising:

a synchronous mirror delay (SMD); and

a phase detector control block in electronic communication with the SMD, wherein the phase detector control block receives a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), the CIN and CDLY signals each having timing characteristics, the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals and the CDLY signal to the SMD, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the SMD to reduce a number of delay stages in the SMD for the selected signal passing through.

14. (previously presented) The memory device of claim 13 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and

a first phase is when $t_{mdl} > t_{ck}/2$;

a second phase is when $t_{mdl} < t_{ck}/2$;

a third phase is when $t_{mdl} = t_{ck}$; and

a fourth phase is when $t_{mdl} = t_{ck}/2$.

15. (previously presented) The memory device of claim 14 wherein when $t_{mdl} < t_{ck}/2$ the number of delay stages in the SMD is comparable to when $t_{mdl} > t_{ck}/2$.

16. (previously presented) The memory device of claim 14 wherein the number of delay stages when $t_{mdl} < t_{ck}/2$ is reduced by substantially one-half.

17. (previously presented) The memory device of claim 14 wherein the number of delay stages when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

18. (currently amended) ~~A synchronous mirror delay system, comprising:~~

~~a synchronous mirror delay (SMD); and~~

~~a phase detector in electronic communication with the SMD and comprising:~~

~~means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and CDLY each having timing characteristics; and~~

~~means for outputting a pair of branches each having a logical level, the logical levels of the branches defining a plurality of conditions based on the timing characteristics of CIN and CDLY~~

~~wherein for at least one of the plurality of conditions, the system comprises means for reducing a number of delay stages for a selected signal to pass through the SMD based on one of the plurality of conditions, the timing characteristics define a period of CIN as t_{clk} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and the plurality of conditions include:~~

~~a first phase when $t_{mdl} > t_{clk}/2$;~~

~~a second phase when $t_{mdl} < t_{clk}/2$;~~

~~a third phase when $t_{mdl} = t_{clk}$; and~~

~~a fourth phase when $t_{mdl} = t_{clk}/2$;~~

~~means for reducing the number of delay stages in the second; and~~

~~means for CIN to bypass the SMD in the third and fourth phases.~~

A synchronous mirror delay system, comprising:

a synchronous mirror delay (SMD); and

a phase detector control block in electronic communication with the SMD,

wherein the phase detector control block receives a clock input signal (CIN), an

inverted clock input signal (CIN'), and a clock delay signal (CDLY), the CIN and CDLY signals each having timing characteristics, the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals and the CDLY signal to the SMD, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the SMD to reduce a number of delay stages in the SMD for the selected signal passing through, the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and the plurality of conditions include:

a first phase when $t_{mdl} \geq t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$;

wherein the phase detector control block selects the selected signal such that the number of delay stages in the second phase is reduced and the selected signal is the CIN signal bypassing the SMD in the third and fourth phases.

19. (currently amended) ~~A synchronizing circuit for use with an integrated circuit, comprising:~~

~~an input buffer comprising means for receiving an external clock signal to produce a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), each having timing characteristics;~~

~~a synchronous mirror delay (SMD) having a measurement delay line input for connection to a measurement delay line, a measurement delay line output connected to a variable delay line input for connection to a variable delay line, the variable delay line including a variable delay line output; and~~

~~a phase detector disposed between the input buffer and the SMD, the phase detector having a first input means for receiving the CIN, a second input means for receiving the CDL, means for generating one of a plurality of output signal combinations, each combination corresponding to a phase of the CIN and CDLY signals based on the timing characteristics, means for connecting a CDLY SMD input to the measurement delay line input, means for connecting a SMD output connected to the variable delay line output, and a circuit selectively inputting CIN or CIN' as a CIN SMD input based on the phase of the signals, wherein for at least one of the phases, a number of delay stages is reduced for the external clock signal to pass through the SMD.~~

A synchronizing circuit for use with an integrated circuit, comprising:

an input buffer for receiving an external clock signal to produce a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), each having timing characteristics;

a synchronous mirror delay (SMD) having a measurement delay line input, a variable delay line input, and a variable delay line output; and

a phase detector control block disposed between the input buffer and the SMD, the phase detector having a first input for receiving the CIN, a second input for receiving the CDLY and a third input for receiving the CIN', wherein the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals to the variable delay line input and the CDLY signal to the measurement delay line input, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the variable delay line input to reduce a number of delay stages in the SMD for the external clock signal passing through.

20. (previously presented) The circuit of claim 19 wherein the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and when $t_{mdl} < t_{ck}/2$, CIN' is input into the SMD and when $t_{mdl} > t_{ck}/2$ CIN is input into the SMD.

21. (previously presented) The circuit of claim 20 wherein the number of delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced.

22. (previously presented) The circuit of claim 20 wherein the number of delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

23-25. (canceled)

26. (currently amended) ~~A system, comprising:~~

~~a phase detector comprising means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), each signal having timing conditions, and means for generating a plurality of output signal combinations, each combination based upon the timing conditions; and~~

~~logic in electronic communication with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals;~~

~~wherein the system selectively feeds CIN or an inverted clock input signal (CIN') into a synchronous mirror delay ("SMD") based upon the plurality of output signal combinations to reduce a number of delay stages for a selected signal to pass through the SMD.~~

A system, comprising:

a synchronous mirror delay (SMD); and

a phase detector control block in electronic communication with the SMD, wherein the phase detector control block comprises a phase detector, a logic circuit, and multiplexers, wherein the phase detector control block receives a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), the CIN and CDLY signals each having timing characteristics, the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals and the CDLY signal to the SMD, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the SMD to reduce a number of delay stages in the SMD for the selected signal passing through.

27. (previously presented) The system of claim 26 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and the phases include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$.

28. (previously presented) The system of claim 27 wherein the number of delay stages is reduced.

29. (previously presented) The system of claim 27 wherein the number of delay stages is reduced substantially by one-half.

30. (previously presented) The system of claim 27 wherein the number of delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

31-33. (canceled)

34. (currently amended) ~~A system, comprising:~~

~~a processor;~~

~~a memory controller;~~

~~a plurality of memory devices;~~

~~a first bus interconnecting the processor and memory controller;~~

~~a second bus interconnecting the memory controller and the plurality of memory devices;~~

~~each of the memory devices having:~~

~~a synchronous mirror delay (SMD);~~

~~a phase detector comprising means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), each signal having timing conditions including a period of CIN (t_{clk}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}); and means for generating a plurality of output signal combinations, each combination corresponding to phases of the signals based upon the timing conditions; and~~

~~logic in electronic communication with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals to input CIN into the SMD when $t_{mdl} > t_{clk}/2$ and input CIN' into the SMD when $t_{mdl} < t_{clk}/2$ to reduce a number of delay stages in the SMD.~~

A system, comprising:

processor;

a memory controller;

a plurality of memory devices;

a first bus interconnecting the processor and memory controller;

a second bus interconnecting the memory controller and the plurality of memory devices;

each of the memory devices having;

a synchronous mirror delay (SMD); and

a phase detector control block in electronic communication with the SMD, wherein the phase detector control block comprises a phase detector, a logic circuit, and multiplexers, wherein the phase detector control block receives a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), the CIN and CDLY signals each having timing characteristics, the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals and the CDLY signal to the SMD, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the SMD to reduce a number of delay stages in the SMD for the selected signal passing through.

35-81. (canceled)